## CLAIMS

What is claimed is:

1. An apparatus comprising:

a data alignment device including

a plurality of input channels to receive a stream of input characters;

a control code detector coupled to the plurality of input channels to detect the occurrence of an aligning character in each input channel;

a plurality of buffers, each buffer coupled to one input channel to store the input characters received over that input channel;

a plurality of output channels, each output channel coupled to one buffer and to a corresponding input channel to transmit a stream of characters from the corresponding buffer; and

a control unit coupled to the control code detector and buffers, and configured to monitor the occurrence of an aligning character in each input channel, to hold the aligning character and subsequently received input characters for each input channel in the corresponding buffer until an aligning character has been detected on every input channel, then resume transmissions over all of the output channels starting with each aligning character on the corresponding buffers and then the subsequently received input characters in the order in which they were received.

2. The apparatus of claim 1 wherein the control unit is configured to generate filler characters and transmit them over those output channels where an aligning character has been detected on its corresponding input channel.

3. The apparatus of claim 1 wherein the control unit to stop generating and transmitting the filler characters once an aligning character has been detected on every input channel.

4. The apparatus of claim 1 wherein the plurality of buffers are configured as first-in, first-out stacks.

5. The apparatus of claim 1 wherein transmissions over the plurality of output channels includes digital transmissions.

6. The apparatus of claim 1 further comprising:
an output clock to transmit one character over each output channel on each clock cycle.

7. The apparatus of claim 1 wherein the control unit to stop holding the aligning character and subsequently received input characters for each input channel in the corresponding buffer if an aligning character has not been detected on every input channel within a given period of time from the first detected aligning character.

8. The apparatus of claim 1 wherein the control unit stops holding the aligning character and subsequently received input characters for each input channel in the corresponding buffer if an aligning character has not been detected on every input channel within a given number of characters from the first detected aligning character.

9. The apparatus of claim 1 wherein the aligning character is the character /A/.

10. The apparatus of claim 1 wherein the filler character is the character /R/.

11. The apparatus of claim 1 further comprising:

a rate matching device including

a plurality of input channels coupled to the plurality of output channels of the data alignment device to receive the output stream of characters from the data alignment device;

a buffer coupled to the plurality of input channels to store the characters received over the input channels of the rate matching device;

a plurality of output channels coupled to the buffer and each output channel corresponding to one input channel of the rate matching device to transmit a stream of characters from the buffer; and

a control unit coupled to the buffer and configured to control the transmission of characters from the buffer, insert a filler character if an underflow condition is detected, and remove a filler character if an overflow condition is detected.

12. The apparatus of claim 11 further comprising:

a data counter to monitor the number of data stored in the rate matching buffer at any one time.

13. The apparatus of claim 11 wherein the buffer for the rate matching device is configured as a first-in, first-out buffer stack with six storage elements.

14. The apparatus of claim 11 further comprising:

a control code detector for the rate matching device coupled to the plurality of input channels to detect the occurrence of an aligning character in each input channel for the rate matching device before initiating the transmission of characters from the buffer.

15. The apparatus of claim 11 wherein the control unit for the rate matching device only removes or inserts the filler character during the interval between two data packets.

16. The apparatus of claim 11 wherein the buffer for the rate matching device comprises one buffer for each input channel to the rate matching device.

17. The apparatus of claim 11 wherein the control unit of the rate matching device does not begin to transmit characters from the rate matching buffer until a plurality of characters have been stored in the rate matching buffer.

18. The apparatus of claim 11 wherein the transmission of characters from the rate matching buffer is synchronous over all output channels for the rate matching device.

19. The apparatus of claim 11 wherein the apparatus comprises an integrated circuit device.

20. A method comprising:

aligning one or more transmission channels including,

detecting the occurrence of an aligning character in a plurality of input channels;

stalling the retransmission of the aligning character and the subsequently received characters for each transmission channel where an aligning character has been received until an aligning character has been detected on every input channel; and

transmitting the stalled characters, starting with the aligning characters and continuing with the subsequently received characters once an aligning

character has been received on every input channel.

21. The method of claim 20 wherein first received characters are transmitted first.

22. The method of claim 20 wherein transmitting the stalled characters comprises transmitting synchronously over all output channels.

23. The method of claim 20 further comprising:

buffering the aligning character and subsequently received characters for each input channel in a buffer until an aligning character has been detected on every input channel.

24. The method of claim 23 further comprising:

resetting the buffer if an aligning character is not detected in every input channel within a maximum number of characters from the first received aligning character in any input channel.

25. The method of claim 20 wherein the aligning character is the character /A/.

26. The method of claim 20 further comprising:

transmitting one or more filler characters over an output channel corresponding to an input channel on which an aligning character has been detected until an aligning character has been detected in every input channel.

27. The method of claim 26 wherein the filler character is the character /R/.

28. The method of claim 20 further comprising:

matching the transmission rates of a first clock to the transmission rates of a second clock including,

receiving one or more characters over a plurality of input channels synchronized by the first clock;

buffering the characters received;

transmitting the one or more buffered characters over one or more output channels synchronized by the second clock;

inserting a filler character in each output channel if an underflow condition is detected; and

removing a filler character in each output channel if an overflow condition is detected.

29. The method of claim 28 wherein matching the transmission rates further comprises:

awaiting the synchronous detection of an aligning character in each input channel before initiating the transmission of characters from the buffer.

30. The method of claim 28 wherein matching the transmission rates removing and inserting the filler character only occurs during the interval between two data packets.

31. The method of claim 28 wherein transmission of buffered characters does not begin until a plurality of characters have been buffered.

32. The method of claim 28 wherein the transmission of the buffered characters is synchronous over all output channels for the rate matching device.

33. A channel alignment system comprising:

means for detecting the occurrence of an aligning character in a plurality of input channels;

means for stalling the retransmission of the aligning character and the subsequently received input characters for each input channel where an aligning character has been received until an aligning character has been detected on every input channel; and

means for transmitting the stalled characters, starting with the aligning characters and continuing with the subsequently received characters, once an aligning character has been received in every input channel.

34. The channel alignment system of claim 33 further comprising:

means for buffering the aligning character and subsequently received input characters for each input channel in a buffer until an aligning character has been detected in every input channel.

35. The channel alignment system of claim 34 further comprising:

means for resetting the buffer if an aligning character is not detected in every input channel within a maximum number of characters from the first received aligning character in any input channel.

36. The channel alignment system of claim 33 further comprising:

means for transmitting one or more filler characters over an output channel corresponding to an input channel on which an aligning character has been detected until an aligning character has been detected in every input channel.

37. The channel alignment system of claim 36 further comprising:

means for synchronously transmitting over all output channels.

38. A rate matching system comprising:
means for receiving one or more characters over a plurality of input channels synchronized by a first clock;
means for transmitting the one or more received characters over one or more output channels synchronized by a second clock; and
means for inserting a filler character in each output channel if an underflow condition is detected.

39. The rate matching system of claim 38 further comprising:
means for buffering the characters received.

40. The rate matching system of claim 38 further comprising:
means for removing a filler character in each output channel if an overflow condition is detected.

41. The rate matching system of claim 40 wherein an underflow condition occurs when the second clock is faster than the first clock.

42. The rate matching system of claim 38 wherein an overflow condition occurs when the first clock is faster than the second clock.

43. An integrated circuit device for aligning communication channels comprising:
a control code detector to detect aligning codes in a plurality of transmission channels;
a plurality of buffers to store the data from the transmission channels; and
a control unit coupled to the control code detector and buffers, and configured to monitor the occurrence of aligning codes, to hold the aligning codes until aligning codes have been detected in all transmission channels, then synchronously

transmit the content of the buffers starting with the aligning codes.

44. The integrated circuit device of claim 43 wherein the control unit is configured to generate and transmit filler characters until aligning codes have been received over every transmission channel.

45. An integrated circuit device for matching the cycles of two clocks in a communication device comprising:

a buffer to store a plurality of characters received; and

a control unit coupled to the buffer and configured to control the transmission of characters from the buffer, insert a filler character if an underflow condition is detected, and remove a filler character if an overflow condition is detected.

46. The integrated circuit device of claim 45 further comprising a control code detector to detect the occurrence of an aligning codes before initiating the transmission of characters from the buffer.

47. The integrated circuit device of claim 45 wherein an underflow condition is detected when the number of characters in the buffer decreases below a certain minimum number.

48. The integrated circuit device of claim 45 wherein an overflow condition is detected when the number of characters in the buffer increases above a certain maximum number.

49. The integrated circuit device of claim 45 wherein if an underflow condition is detected a filler character is inserted into the buffer.

50. The integrated circuit device of claim 45 wherein if an overflow condition is detected a filler character is removed from the buffer.

51. A method for aligning one or more transmission channels comprising:

detecting the occurrence of an aligning character in a plurality of input channels;

buffering the aligning character and subsequently received input characters for each input channel in a buffer until an aligning character has been detected in every input channel;

stalling the transmission of the aligning character and the subsequently received input characters for each input channel where an aligning character has been received until an aligning character has been detected in every input channel;

transmitting one or more filler characters over an output channel corresponding to an input channel on which an aligning character has been detected until an aligning character has been detected in every input channel; and

transmitting the buffered characters, starting with the aligning characters and continuing with the subsequently received characters, once an aligning character has been received in every input channel.

52. The method of claim 51 wherein first received characters are transmitted first.

53. The method of claim 51 wherein transmitting the buffered characters comprises transmitting synchronously over all output channels.

54. The method of claim 51 further comprising:

resetting the buffer if an aligning character is not detected in every input channel within a maximum number of characters from the first received aligning character in any input channel.

55. The method of claim 51 wherein the aligning character is the character /A/.

56. The method of claim 51 wherein the filler character is the character /R/.

57. A method for matching the transmission rates of a first clock to the transmission rates of a second clock comprising:

receiving one or more characters over a plurality of input channels synchronized by the first clock;

transmitting the one or more received characters over one or more output channels synchronized by the second clock; and

inserting a filler character in each output channel if an underflow condition is detected.

58. The method of claim 57 for matching the transmission rates of a first clock to the transmission rates of a second clock further comprising:

buffering the characters received.

59. The method of claim 57 for matching the transmission rates of a first clock to the transmission rates of a second clock further comprising:

removing a filler character in each output channel if an overflow condition is detected.

60. The method of claim 57 for matching the transmission rates of a first clock to the transmission rates of a second clock further comprising:

awaiting the synchronous detection of an aligning character in each input channel before initiating the transmission of characters from the buffer.

61. The method of claim 57 for matching the transmission rates of a first clock to the transmission rates of a second clock further comprising:

removing and inserting the filler character only occurs during the interval between two data packets.